

FRAUNHOFER INSTITUTE FOR INDUSTRIAL MATHEMATICS





ANALOG CIRCUIT DESIGN – RAPID AND RELIABLE

Analog Insydes – The Intelligent Symbolic Design System For Analog Circuits

Analog Insydes is a Mathematica[®] application package for modeling, analysis and design of analog electronic circuits, tailored specifically for industrial applications. Analog Insydes and Mathematica[®] integrates the following in one environment:

- describe linear and nonlinear circuits and control systems by means of hierarchical netlists
- netlist generation using the graphical Analog Insydes Schematics Creator
- set up circuit equations from netlists in frequency and time domain
- compute transfer functions symbolically
- extract approximated symbolic design formulas
- simulate transient responses of nonlinear dynamic circuits
- use powerful reduction methods generating interpretable symbolic expressions
- analyse symbolically and numerically
- visualize your analysis results with custom graphics functions
- import and export netlists and data to commercial circuit simulators
- document your work with text, formulas, and circuit schematics

With its capability to compute approximated symbolic formulas for circuit characteristics, Analog Insydes is the perfect tool to assist designing complex circuits. Analog Insydes is available for Windows, Linux, and Macintosh platforms.

Read more on Analog Insydes at www.analog-insydes.com

Vertrieb durch: ADDITVE GmbH • Max-Planck-Straße 22b • 61381 Friedrichsdorf http://additive-mathematica.de/ • eShop: http://eshop.additive-net.de Verkauf: +49-6172-5905-134 mathematica@additive-net.de Support: +49-6172-5905-20 support@additive-net.de



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1 Device under test

2 Analog Insydes

Schematics Creator

with two test benches



What's new in Analog Insydes 2012?

Analog Insydes 2012 provides advanced and extended features for designing modern analog circuits. These new capabilities solve challenges intractable by numerical methods and accelerate optimal parameter finding in analog design.

Create Circuit Schematics on Click

Analog Insydes 2012 offers a fast and user-friendly interface to the new Analog Insydes Schematics Creator. Fraunhofer ITWM created this graphical user interface for drawing circuit schematics exclusively for users of Analog Insydes. They can generate and manipulate wiring diagrams of Analog Insydes and custom components. For this purpose, the tool imports existing netlists, models and model cards. Thus, it yields a convenient environment for developing complex behavioral models just on click. The Schematics Creator is freely available at www.analog-insydes.com

Binaries On!

Analog Insydes 2012 introduces fast and handy platform-specific binaries supplementing its specialized numerical solvers. This speeds up all steps of the design flow which depend on simulation results like behavioral model order reduction.

Test Bench Setup

The new concept of multiple test benches for a device under test (DUT) facilitates user friendly switching of test bench layouts. By quickly simulating devices in different setups Analog Insydes generates reduced behavioral models, which are valid for multiple test benches. Also, this allows you to easily export reduced behavioral models in hardware description languages like VHDL.

Identify Sequential Equations

Analog Insydes 2012 helps to benefit from our established sequential equations concept. To improve performance and stability this feature is utilizing structural information encoded by a special equation setup. Now you can instantly apply our improved procedures to custom models without further knowledge of the sequential syntax.

New Model Export Filters

Analog Insydes 2012 adds two new filters for exporting behavioral models to the Spectre[®] Compiled Model Interface (CMI) of Cadence[®] and the hardware description language Verilog-A.

New LTSpice® Import Filter

Analog Insydes 2012 is providing a comprehensive list of netlist import filters, which was extended for reading LTSpice[®] netlists. An extensive library of new device models (like VDMOS or OTA) allows for analyzing analog circuits created using LTSpice[®].